

Cost-effective cleaning and high-quality thin gate oxides

by M. M. Heyns
T. Bearda
I. Cornelissen
S. De Gendt
R. Degraeve
G. Groeseneken
C. Kenens
D. M. Knotter
L. M. Loewenstein

P. W. Mertens
S. Mertens
M. Meuris
T. Nigam
M. Schaekers
I. Teerlinck
W. Vandervorst
R. Vos
K. Wolke

Some recent findings in the area of wafer cleaning and thin oxide properties are presented in this paper. Results are shown for a practical implementation of a simplified cleaning concept that combines excellent performance in terms of metal and particle removal with low chemical and DI-water consumption. The effect of organic contamination on ultrathin gate-oxide integrity is illustrated, and the feasibility of using ozonated DI water as an organic removal step is discussed. Metal outplating from HF and HF/HCl solutions is investigated. Also, the final rinsing step is critically evaluated. It is demonstrated that Si surface roughness without the presence of metal contaminants does not degrade gate-oxide integrity. Finally, some critical remarks on the reliability measurements for ultrathin gate oxides are given; it is shown that erroneous conclusions can be drawn from constant-current charge-to-breakdown measurements.

Introduction

Cleaning is the most frequently repeated step in IC production. The RCA clean, developed in 1965, still forms

the basis for most front-end wet cleans. Over the last few years considerable research effort has been directed toward the development of novel cleaning techniques that are more cost-effective and have a lower environmental impact. The scientific progress made in this area over the last few years is enormous, and at the present time it is fair to state that advances are made through scientific understanding, rather than random experiments or just "pure luck." One of the most critical cleaning steps is the pre-oxidation cleaning, especially for ultrathin oxide growth. Some critical issues on the technology and reliability of the ultrathin gate insulators that have recently attracted attention are the effect of organic contamination and Si surface roughness on the gate-oxide integrity and the validity of constant-current charge-to-breakdown measurements as a reliability test. These issues are discussed in more detail in this paper.

Wet-cleaning roadmap

The RCA clean [1], developed in 1965, still forms the basis for most front-end wet cleans. A typical RCA-type cleaning sequence starts with an SPM step ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) followed by a dip in diluted HF. The SC1 step ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$) removes particles, while the SC2 step ($\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$) removes metal. Despite increasingly stringent process demands and orders-of-magnitude improvements in analytical techniques, cleanliness of

©Copyright 1999 by International Business Machines Corporation. Copying in printed form for private use is permitted without payment of royalty provided that (1) each reproduction is done without alteration and (2) the Journal reference and IBM copyright notice are included on the first page. The title and abstract, but no other portions, of this paper may be copied or distributed royalty free without further permission by computer-based and other information-service systems. Permission to republish any other portion of this paper must be obtained from the Editor.

0018-8646/99/\$5.00 © 1999 IBM

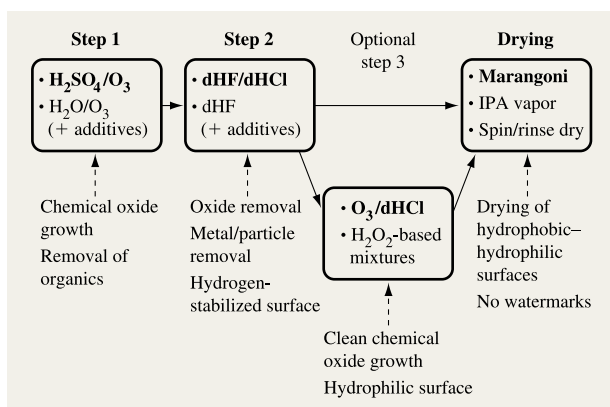


Figure 1

Schematic illustration of the IMEC-clean concept.

chemicals, and DI water, the basic cleaning recipes have remained unchanged since the first introduction of this cleaning technology. Since environmental concerns and cost-effectiveness were not a major issue 30 years ago, the RCA cleaning procedure is far from optimal in these respects. Recently much research effort has been directed toward understanding the cleaning chemistries and techniques.

Important chemical savings can be obtained in an RCA-type cleaning sequence by using diluted chemistries for both the SC1 and SC2 mixtures. In the SC2 mixture the H_2O_2 can be left out completely, since it has been shown that strongly diluted HCl mixtures are as effective in the removal of metals as the standard SC2 solution [2]. An added benefit of using diluted HCl is that at low HCl concentrations particles do not deposit, as has also been observed experimentally [3]. This is because the isoelectric point for silicon and silicon dioxide is between pH 2 and 2.5 [4]. At a pH above the isoelectric point, the wafer surface has a net negative charge, while below it the wafer surface has a net positive charge. For most particles in liquid solutions at pH values greater than 2–2.5, an electrostatic repulsion barrier between the particles in the solution and the surface is formed. This barrier impedes particle deposition from the solution onto the wafer surface during immersion. Below pH 2, the wafer surface is positively charged, while many of the particles remain negatively charged, removing the repulsion barrier and resulting in particle deposition while the wafers are submerged.

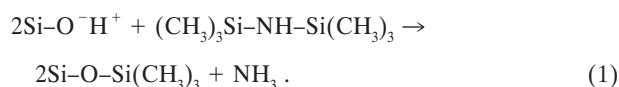
To further lower the chemical consumption during wet wafer cleaning, some simplified cleaning strategies can be used, such as the IMEC clean [5]. The basic concept is summarized in **Figure 1**. In the first step of the IMEC

clean, the organic contamination is removed and a thin chemical oxide is grown. In the second step, the chemical oxide is removed, simultaneously removing particle and metal contamination. An additional third step can be added before final rinsing and drying to make the Si surface hydrophilic to allow for easier drying without the generation of drying spots or “watermarks.” In the Marangoni dryer, the drying is performed by a strong natural force (i.e., the Marangoni effect) in cold DI water, and the wafer is rendered completely dry without evaporation of water or condensation of IPA [6, 7]. Some specific aspects of the various steps are discussed in more detail in the following sections.

Organic contamination removal

In the first step of the IMEC clean, organic contamination is removed. A sufficiently thick chemical oxide must be grown to obtain high particle-removal efficiencies in the second step of the cleaning sequence [5]. Traditional cleaning sequences use sulfuric-acid-based mixtures (such as $\text{H}_2\text{SO}_4/\text{O}_3$) for this purpose, but from an environmental perspective the use of ozonated DI water would be preferable. The use of ozonated DI water further reduces chemical consumption and (even more important) DI-water consumption, since the difficult rinse step after the sulfuric acid bath [8] is avoided. Ozone has been used exhaustively in the field of waste treatment and drinking water sterilization because of its strong oxidizing power. When ozone is dissolved in water, its self-decomposition is accelerated. Although an exact mechanism is not known, it is believed that the decomposition of ozone leads to the generation of OH^* radicals, which are thought to play an important role in decomposing organic material [9, 10]. A potential drawback of ozonated water is the relatively low solubility of ozone in water, which is about 20 ppm at room temperature [11]. The cleaning efficiency of ozonated DI water was evaluated using HMDS (hexamethyldisilazane)-contaminated wafers.

The organic compound HMDS is used in IC processing as a photoresist primer. It reacts with the surface silanol groups as follows:



This reaction is highly selective and converts all silanol groups, leaving a monolayer coverage of TMS (trimethylsiloxane). After the necessary processes are completed, the residue of this compound should also be removed. It is, therefore, a good test material for evaluating the organic removal efficiency of various cleaning solutions. Using time-of-flight SIMS (ToF-SIMS) measurements, it was observed that an SPM ($\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$) or SOM ($\text{H}_2\text{SO}_4/\text{O}_3$) treatment can be

successfully applied for removing organic contamination, more particularly the HMDS residues [12]. The full removal of HMDS using ozonated DI water (**Figure 2**) is more difficult. At room temperature, high ozone concentrations can be obtained in the solution, but the reaction rate is relatively slow, causing an incomplete removal of the HMDS within the experimental time. At elevated temperature the reaction rate is enhanced, but the solubility of the ozone is lower. Temperature is the most important parameter for HMDS removal, but at any temperature, the ozone concentration correlates linearly with the cleaning efficiency. Also, a mild pH effect can be observed at any temperature. Careful optimization of the various parameters of the ozonated DI-water process is therefore needed to obtain a high organic removal efficiency [13].

Metal outplating from HF solutions

The second step of the IMEC clean removes the chemical oxide, simultaneously removing the particle and metal contamination. The mixture and dipping time must be optimized to provide a maximum particle-removal efficiency and low metal-contamination level with only a small amount of thermal oxide loss.¹ It is known that trace amounts of noble-metal ions, such as Ag, Au, and especially Cu, that are present in the HF solution can deposit on the Si surface [14, 15]. It has been reported that in the early stages of copper deposition, the formation of metal nuclei on the wafer surface is the dominating process. After this nucleation period, the metallic copper nuclei grow in size [16]. This deposition process is an electrochemical process that involves mobile charge carriers. Therefore, the silicon semiconductor properties and illumination conditions play an important role in it, especially for Cu [17]. When the wafers are immersed in darkness, the copper surface concentration increases only very weakly with time. Under illumination, however, a strong increase in the copper surface concentration is observed after about 15 s immersion. The p-type and n-type Si wafers show an identical behavior [17]. From these results it can be concluded that copper deposition from dilute aqueous HF solutions on Si surfaces is limited by the minority carrier concentration at the wafer surface [17].

Chloride ions are often present as contaminants in HF. Their addition to the Cu-contaminated HF solution drastically changes the outplating of Cu (**Figure 3**). The large effect of the illumination condition disappears and a strong dependence on the HCl concentration is observed [18]. The addition of chloride can suppress the effect of illumination. Small amounts of chloride increase the copper deposition owing to the catalyzing effect of the

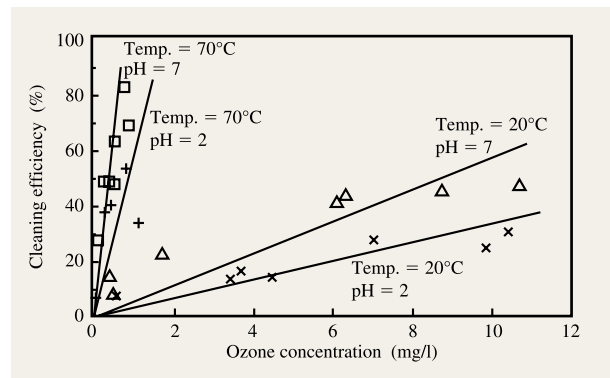


Figure 2

Cleaning efficiency for HMDS-contaminated wafers vs. ozone concentration, temperature, and pH for an immersion time of 60 s. The pH of the solution was controlled by the addition of HCl. The straight lines (assuming no cleaning action when ozone is not present) are for illustrative purposes only.

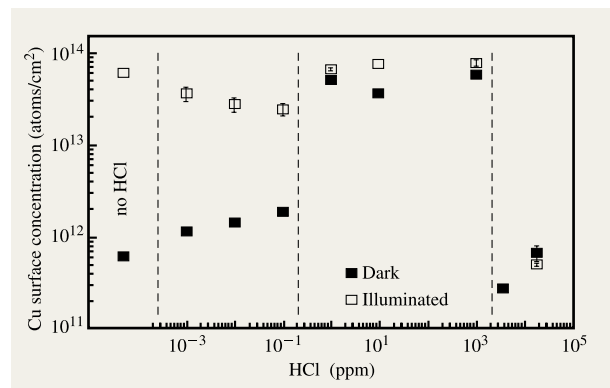


Figure 3

Copper surface concentration as a function of HCl addition in darkness and under illumination after a 5-min dip in a 0.5% HF solution containing 100 w-ppb of copper ions. Identical results are found for n-type and p-type wafers.

chloride ions on the $\text{Cu}^{2+}/\text{Cu}^+$ reaction. Large amounts of added chloride suppress the copper deposition by the formation of soluble higher cuprous chloride complexes. The optimized HF/HCl mixture provides protection against metal outplating from the solution, and in combination with an optimized *in situ* monitoring technology [19] it allows the useful bath lifetime to be significantly prolonged, thereby dramatically lowering the HF waste. The bath lifetime can be extended even further by using point-of-use purification [20].

¹ M. Meuris, I. Cornelissen, and M. Heyns, internal IMEC report, 1995.

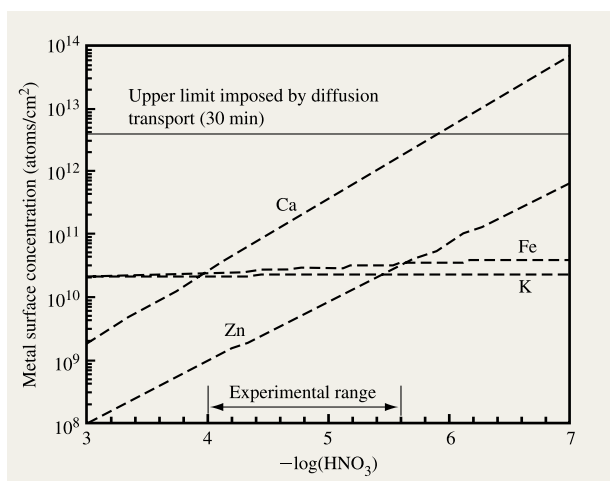


Figure 4

First-order model obtained from a designed experiment for the metal surface concentration obtained from overflow rinsing in an acidified solution containing 5×10^{-8} mol/l of each of the four metals, at 3 l/min at a temperature of 20°C and a rinse time of 30 min. The experimental range which was used for the design of experiments is indicated in the graph. The lines outside this region are extrapolations from the model.

Reoxidation and final rinsing

An additional third step can be added to the cleaning sequence in order to make the Si surface hydrophilic. This allows for easier drying without the generation of drying spots or watermarks. Optimized ozonated mixtures, such as diluted HCl/O₃ (or dHCl/O₃), can be used to make the Si surface hydrophilic at low pH values in order to avoid the reintroduction of metal contamination. Advanced CMOS technologies require the growth of very thin gate insulators with precise thickness control. Therefore, the effect on the oxide thickness control of the presence of the chemical oxide prior to oxidation was investigated in more detail. It was found that the presence of a thin chemical oxide (estimated thickness 0.6 to 0.8 nm) on the Si surface prior to oxidation does not significantly influence the final oxide thickness or the thickness variation over the wafer when a clustered oxidation and poly-Si deposition process is used [21]. In this cluster the ambient during loading and heating can be very well controlled. On wafers which received a wet HF dip immediately before loading, a thin thermal oxide of about 1.17 nm is grown during ramp-up to 650°C in diluted oxygen, while on an SC2-last wafer, an oxide thickness of 1.21 nm is measured after this treatment. A 30-min oxidation at 800°C in 10% diluted oxygen on an HF-last and an SC2-last wafer resulted in an average oxide thickness of 2.34 nm and 2.42 nm, respectively, with a

thickness uniformity (3σ variation over the wafer) of 0.03 nm. A similar oxidation procedure using a standard nonclustered furnace resulted in an average oxide thickness of 2.96 nm with a 3σ variation of 0.21 nm. This illustrates the importance of having good control of the ambient conditions during loading and ramping. In terms of electrical performance and defect density, no significant differences were found between the HF-last and SC2-last samples, provided that the metal and particle contamination after these cleaning procedures was sufficiently low.

The final surface concentration of metals after cleaning, particularly of Ca, is strongly determined by the final rinsing [22, 23]. The behavior of metal surface deposition during final rinsing was therefore studied in more detail using a designed experiment [24]. The wafers were dried immediately by pulling them out of the rinsing solution into an IPA vapor. The variables investigated included the concentration of added HNO₃, the temperature, the rinse time, and the final clean applied prior to rinsing. Calcium shows a pronounced tendency to deposit on the wafer surface. This is especially important in view of the strong effect of Ca contamination on the gate-oxide integrity [25]. The dominant experimental effect was the reduction of the Ca surface concentration with increasing concentration of HNO₃ added to the rinse water. The second most important effect is the reduction of the Ca surface concentration if the final clean is changed from SC1 to SC2. Because of the carry-over layer [26], this effect is more than likely due to the same mechanism as the HNO₃ spiking, i.e., the change in pH of the solution. This reveals a potential pitfall for the implementation of dilute chemistries without sufficient understanding. Indeed, if a concentrated SC2 solution is replaced with a very dilute HCl treatment prior to the final rinse, the initial pH during the final rinse is accordingly higher. This in turn results in increased metal deposition on the wafer surface due to a faster ion exchange at the chemical oxide surface. It was found that with increasing rinse time the metal surface concentration increases, indicating the existence of transport-limited surface deposition in the experiments. This may also reveal a practical pitfall for extended rinse cycles and illustrates that, especially for rinsing after dilute HCl treatments, the rinse times should be kept as short as possible. An increase in the temperature was found to result in a lower Ca surface concentration.

Figure 4 shows the surface deposition for different metals calculated from the competitive adsorption model as a function of the concentration of HNO₃ spiking [27, 28]. The Ca surface concentration indeed shows a very strong pH dependence. In this figure, the upper limit imposed by diffusive transport is indicated. In agreement with the time dependence mentioned above, one can see

Table 1 Typical implementation of the IMEC clean concept in an automated wet bench.

Step 1	H ₂ SO ₄ /O ₃ Three quick dump rinses (QDR, hot/cold)	90°C 60°C/20°C	5 min 8 min
or Step 1*	O ₃ /DI water	Optimized conditions	
Step 2	dHF (0.5%) /dHCl (0.5M)	22°C	2 min
Step 3	Final rinse + O ₃ /HCl (megasonic energy)	20°C	10 min
Drying	Marangoni drying (with HCl spiking)	20°C	8 min
Total cleaning time			32 min

Table 2 Final metal contamination on intentionally contaminated wafers after either an IMEC clean or an optimized RCA cleaning sequence (SPM–dHF–hot SC1–SC2–rinse/dry).

Contaminant	Metal concentration on the wafer (10 ¹⁰ atoms/cm ²)			
	Ca	Fe	Cu	Zn
Initial concentration	154.4	5.6	4.4	1.8
Modified RCA clean	<0.26	0.2	0.4	0.2
IMEC clean	<0.26	0.1	<0.07	0.08

that the higher values obtained in the experimental range are indeed limited by diffusion transport. Therefore, the equilibrium concentration of Ca may even be higher than that given by the fit model.

IMEC-clean results

The IMEC clean was implemented in an automated wet bench, and its performance was compared to that of an optimized RCA clean, using a hot SC1 bath. The IMEC-clean recipe used during the tests is summarized in **Table 1**. The most striking overall result is that very low final metal-contamination levels were consistently obtained with this clean. Typical results revealed metal-contamination levels below the detection limit of the vapor-phase decomposition–droplet surface etching–total reflectance X-ray fluorescence (VPD–DSE–TXRF) technique, which is lower than 10⁹ atoms/cm² for most metals of interest. These results were obtained using standard 1-ppb-grade chemicals. Also, low final metal-contamination levels were observed on intentionally contaminated wafers. This is shown in **Table 2** for wafers contaminated with Ca, Fe, Cu, and Zn from an SC1-type solution and subsequently cleaned with either an IMEC clean or a modified RCA cleaning sequence containing a hot SC1 step.

Particle-removal efficiency was tested in detail by using intentionally contaminated wafers. Various types of particles (Si₃N₄, Al₂O₃, SiO₂) were tested on various substrate types (silicon, TEOS oxide, thermal oxide, nitride). Initial particle counts varied between 1500 and

2500 particles per wafer, with average particle sizes between 0.15 μm and 0.3 μm. The most difficult case is the removal of nitride particles from a nitride surface. In that case a relatively important statistical spread was found on the particle-removal efficiency, which varied between 80 and 100%. For all other combinations, very high particle-removal efficiencies in the range of 98–100% were obtained. About 3.2 nm of thermal oxide was removed during the IMEC clean, which is comparable to the etching in typical RCA cleaning sequences using heated SC1 solutions.

Capacitor structures with poly-Si gates and gate-oxide thicknesses varying from 1.5 to 10 nm were fabricated in order to investigate gate-oxide integrity after the IMEC clean and the modified RCA clean. The oxidations were performed in a clustered batch furnace. No Cl-containing species that could mask the effects of low levels of contamination were used in the oxidation ambient. The wafers were 6 in. in size, and the largest capacitor area available was 16 mm². This gives a lower limit for the defect densities that can be observed with sufficient statistical significance of approximately 0.1 defect/cm². The defect densities measured at 12 MV/cm in a ramp breakdown test were for both cleans consistently below or close to this detection limit, and no statistically significant difference could be observed between the two cleaning methods over a number of runs for various oxide thicknesses. More detailed measurements of the charge to breakdown confirmed these results. This illustrates that the IMEC clean can be used as a cost-effective

Table 3 Overview of the experimental conditions used to study the effect of organic contamination and wafer storage during poly-Si/SiO₂/Si stack formation on gate-oxide integrity.

Condition	Treatment
A	Minimum time between cleaning, oxidation, and poly-Si deposition
B	Wafers 72 hours in box between oxidation and poly-Si deposition
C	Wafers 62 hours in cluster between cleaning and oxidation
D	Wafers 48 hours in cluster between oxidation and poly-Si deposition
E	HMDS monolayer on oxide before poly-Si deposition

replacement for the RCA clean, with the advantage of a much lower chemical consumption and lower footprint of the cleaning tool [29].

Organic contamination

So far, the impact of organic residue contaminants on IC processing is poorly understood, because a variety of contaminants exist (e.g., human skin oils, clean-room air, pump oil, silicone vacuum grease, photoresist, cleaning solvents), and each has a different degree of impact on IC manufacturing. A potential problem is the presence of organic films on wafer surfaces, preventing cleaning solutions from reaching the surface. Therefore, removal of organic contamination is often the first step in cleaning. Recently organic contamination was also identified as a possible origin of a degraded gate-oxide quality [30–32]. Organic pickup during IC processing is hard to avoid. Transport of wafers in plastic boxes results in potential organic contamination. Various process steps can be clustered in vacuum tools, but Si surfaces handled in a vacuum environment are vulnerable to organic contamination.

To investigate the effect of organic contamination and the methods to remove it, three types of organic contamination were used: chemically bound to the surface (HMDS priming); physically adsorbed from exposure to an antistatic polypropylene wafer box; or storage in a vacuum cluster [33]. An overview of the different experimental conditions is given in **Table 3**. All wafers received a standard RCA clean followed by an HF dip (2 min in 1% HF) and a 5-min overflow rinse and Marangoni drying. Reference wafers (condition A) were processed with minimal delay time between cleaning, oxidation, and poly-Si deposition. The impact of organics prior to oxidation was evaluated after prolonged storage in a vacuum cluster (condition C). For the other conditions, organic contamination was applied after oxidation but prior to poly-Si deposition. The time between cleaning and oxidation was kept minimal, and a 5-nm dry oxide was grown. To simulate the effect of larger amounts of organic contamination, some wafers were primed with hexamethyldisiloxane (HMDS), which reacts chemically with surface silanol groups (condition E). It was checked

that neither particle nor metal contamination increased during the storage. It should be stressed, however, that the 5-nm gate-oxide ramp-up and oxidation conditions were selected to enhance the detrimental effects of adsorbed organic contamination, since the temperature ramp-up from vacuum to atmospheric pressure is performed in a low-oxygen-containing ambient.

The result of charge-to-breakdown (Q_{BD}) measurements on the various wafers is shown in **Figure 5**. Three wafers were tested for each condition. The Q_{BD} measurements show no difference in the intrinsic oxide breakdown part of the distribution, but the extrinsic tail is influenced by the different treatments. Storing the wafers in a box between oxidation and poly-Si deposition (condition B) has no important negative effect on the oxide yield. A significant negative effect is observed when the wafers are stored in a vacuum prior to processing (condition C). This negative effect is strongly enhanced owing to the low oxygen content during ramp-up used in this experiment. Poly-Si deposition occurs in a nonoxidizing ambient, thus significantly enhancing the effect of vacuum exposure (condition D). In addition, the strong detrimental effect of the HMDS layer on the oxide yield and reliability (condition E) confirms that the presence of organic contamination is likely responsible for the extrinsic defects in the thin oxide layer. In general, it can be concluded that vacuum exposure before oxidation is less detrimental to the integrity of the 5-nm oxide than exposure after oxidation, and good control of the SiO₂/poly-Si interface is needed.

Effect of Si surface roughness on gate-oxide integrity

Si surface roughness has received much attention over the last few years as a possible cause of gate-oxide defects. When an HF-treated Si surface is heated in an ultraclean Ar ambient, the Si microroughness is increased by thermal etching, which was believed to be detrimental for the thin-gate-oxide breakdown [34]. However, the reduced gate-oxide integrity can also be attributed to the presence of organic contamination on the Si wafer and the formation of SiC on the Si surface at high temperatures [35]. It was recently reported that as far as yield loss is concerned,

silicon surface roughness for very thin oxides (<6 nm) appears to be negligible [36–39], at least at moderate levels of surface roughening. The use of BHF etching to generate an increased Si surface roughness from 0.2 to 0.6 nm rms [40] or etching in dilute ammonia to generate roughness levels up to 9 nm [41] showed no significant effect of the roughness on the breakdown or reliability of thin thermal oxide layers under conditions in which an IMEC clean was used to eliminate the effect of metal contamination and avoid effects of chemical preconditioning.

In view of these results, the SC1 yield loss due to local roughening, as reported previously [42, 43], and the relationship among Si surface roughness, metal contamination, and oxide defects were reevaluated. It has been observed [42, 43] that immersion of hydrophobic wafers into a metal-contaminated SC1 bath (vigorous decomposition of the peroxide) has a direct impact on silicon surface microroughness (small spikes on wafer surface), denoted as clustered light-point defects (LPDs). This observation was explained from a micromasking effect through small oxygen bubbles sticking on the initially hydrophobic surface and thus shielding the surface from the etching action of the SC1 chemistry (with the observed spikes believed to be silicon). Additionally, it was demonstrated that a correlation exists between the spike patterns and resulting breakdown (E_{BD}) data, with an additional SC2 clean being unable to recover the metal-contaminated SC1-induced yield loss [42, 43].

After an initial HF-last clean, wafers were treated in SC1 solutions (1/1/5 at 70°C) spiked with varying amounts of iron (i.e., blank, 0.1 ppb, and 1 ppb), resulting in wafer-surface iron levels between low 10^{10} atoms/cm² for blank SC1 solutions and a few times 10^{12} atoms/cm² for the 1-ppb iron-spiked solution. Subsequently, wafers were treated in a dHF/dHCl bath (diluted HF/diluted HCl), a dHCl bath, or an SC2 solution, all at room temperature. The dHF/dHCl treatment could successfully reduce the iron concentration to levels below the detection limit of VPD–DSE–TXRF (less than 10^9 atoms/cm²), while the dHCl and SC2 clean left a measurable iron content behind (in the range of 10^{10} – 10^{11} atoms/cm²). The wafers were finally treated in a clean SC1 solution in order to exclude the influence of surface conditions on gate-oxide integrity, and oxides with a thickness of 5 nm were grown at 800°C in a dry O₂ ambient.

Immersion of the hydrophobic wafers into an (iron-catalyzed) decomposing SC1 solution resulted in the formation of clustered LPDs, as evidenced by light-scattering plots. **Figure 6** depicts an atomic force microscopy (AFM) plot that shows the shape of typical roughness found on spots with clustered LPDs. After a dHF/dHCl cleaning sequence, the clustered LPDs remained visible on the wafer surface. The results indicated that the overall surface

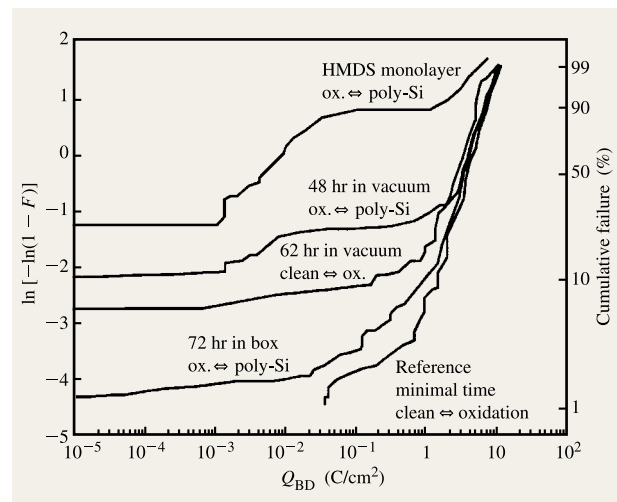


Figure 5

Q_{BD} distributions of 5-nm oxide for the various experimental conditions explained in Table 3. Three wafers with capacitor areas of 1.257×10^{-3} cm² were used for each condition, and the stress condition was 0.1 A/cm² (substrate injection). Typically 120 capacitors were measured on each wafer. The Weibull distribution is given by $\ln[-\ln(1-F)]$, with F being the cumulative failure rate.

roughness as determined with light-scattering techniques is not affected by the SC1 iron content in the range studied. It can be seen from Figure 6 that the clustered LPDs are typically ring-shaped (3–8 μ m in diameter, 2–5 nm deep), while a steep rim (3–8 nm high) is observed on one side of almost every ring. This rim is formed at the lower side of the ring with respect to the orientation of the wafers in the SC1 bath [44, 45]. It has been proposed that this rim is formed by the deposition of the reaction products of the Si etching, which are transported by gravitation to one side of the etch region [44].

Results on gate-oxide integrity are shown in **Figure 7**. Considering the condition with clean SC1 as the reference condition, it can be seen that the wafers treated in the 0.1-ppb-Fe-contaminated SC1, with SC1-related LPDs and iron contamination at the sub- 10^{11} -atoms/cm² levels, have a reduced yield. A treatment in 1-ppb-contaminated SC1, resulting in an iron concentration of about 1.10^{12} atoms/cm², causes a complete yield kill of all capacitors. Worth noting, however, is the effect of a subsequent dHF/dHCl cleaning step. This treatment reduced the iron concentration to 10^9 -atoms/cm² levels and recovered within statistical variation nearly all yield loss induced by the iron-contaminated SC1 treatment, while evidence for clustered LPDs remained clearly visible. Combination of the particle, roughness, and metal data with the capacitor yield information allows us to conclude that capacitor

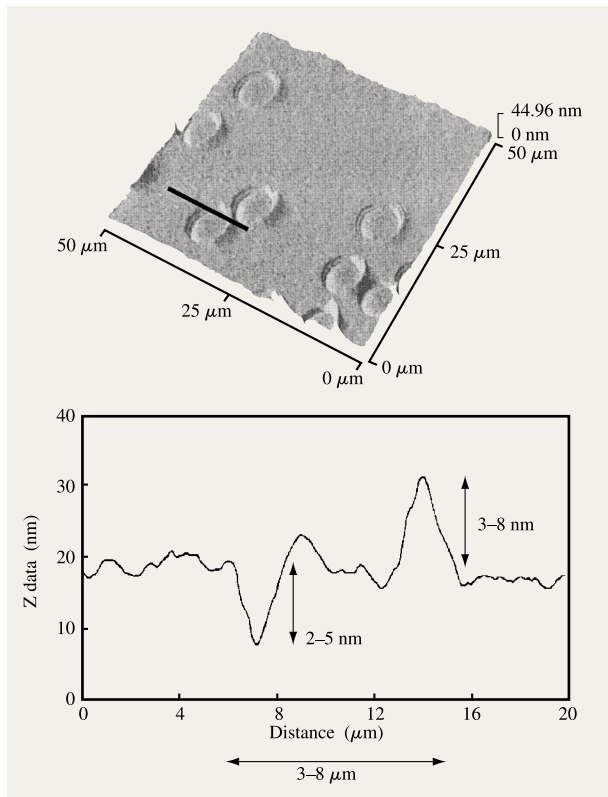


Figure 6

AFM plot of silicon surfaces after immersion of hydrophobic wafers into a 3-ppb-iron-contaminated 1/1/5-by-volume SC1 solution.

yield loss is correlated primarily to the surface iron concentration present after iron-contaminated SC1 treatments, and less to the presence of so-called clustered LPDs as observed by light scattering. Therefore, it is believed that in this case the SC1-induced yield loss is probably due not to the observed silicon surface roughening, but rather to locally high levels of iron contamination which become built in to the SC1-grown chemical oxide.

Reliability measurements on thin oxide layers

The constant-current stress charge-to-breakdown test ($CCS-Q_{BD}$) tool is widely used to evaluate the influence of various processing conditions on the reliability of MOS structures. In such studies it is always assumed that variations of the median value of Q_{BD} are entirely ascribed to the variations of processing conditions. However, for decreasing oxide thickness, Q_{BD} becomes a stronger function of nontechnological parameters such as test structure area, stress current, and polarity. The impact of this observation on the validity of $CCS-Q_{BD}$ measurements

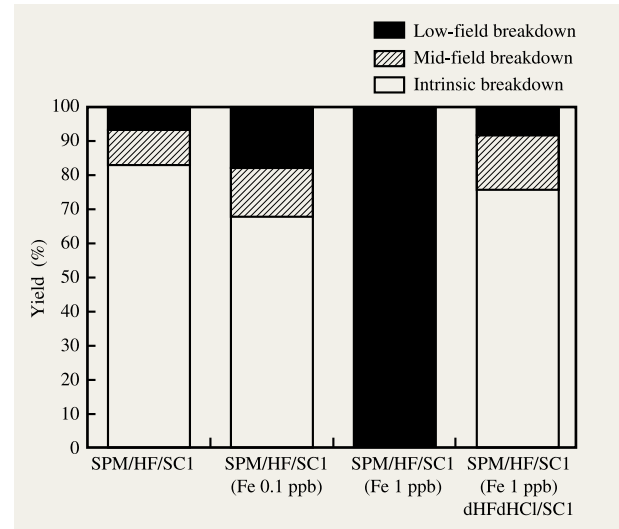


Figure 7

Ramped voltage E_{BD} average yield for low-field (<2 MV/cm), mid-field ($2 \text{ MV/cm} < x < 11 \text{ MV/cm}$) and intrinsic ($>11 \text{ MV/cm}$) breakdown for 15.8-mm^2 capacitors made with 5-nm gate oxides on p-Cz wafers after various pretreatments. Similar results were obtained on n-Cz and epi-pp⁺ wafers.

for the quantification of the reliability of different MOS processes was studied in detail [46].

It was observed that there is an increasing area dependence of Q_{BD} when the oxide becomes thinner. This is a purely statistical effect, due to a decrease of the Weibull slope β with decreasing oxide thickness [47, 48]: The slope of Q_{BD} vs. area is inversely proportional to the Weibull slope β . This decrease in Weibull slope is related to a drop in the critical oxide trap density at breakdown for thinner oxides [47]. Another consequence of the Q_{BD} area dependence becomes visible when the Weibull slope of the Q_{BD} distribution depends on the processing conditions, e.g., where conventional oxides were compared with oxides grown in N_2O . Depending on the capacitor area used for the test, either an improvement or a degradation of the reliability could be observed for N_2O oxides. This is shown in **Figure 8**, where the Q_{BD} distributions of a conventional oxide are compared to those of an oxide grown in pure N_2O ($t_{ox} = 7 \text{ nm}$) for two capacitor areas. Focusing on distributions C and D, one could conclude that the nitridation improves the oxide reliability. However, from distributions A and B, measured on the same wafers but on a different capacitor area, one could conclude the opposite. This is because the nitridation of the oxide decreases $D_{ot,crit}$ and thus reduces the Weibull slope β [49]. This drop in β explains the enhancement of the area dependence for the nitrided oxides.

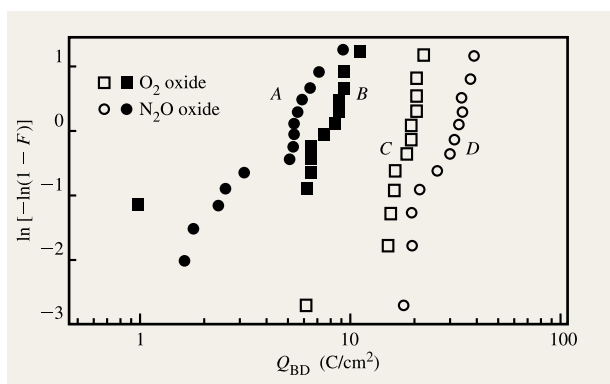


Figure 8

Q_{BD} distribution ($J = +0.1 \text{ A/cm}^2$) for 7-nm conventional oxides and N_2O oxides with two different areas: $5.24 \times 10^{-4} \text{ cm}^2$ (closed symbols), and 10^{-6} cm^2 (open symbols). The Weibull distribution $\ln[-\ln(1-F)]$, with F being the cumulative failure rate, is used to present the data.

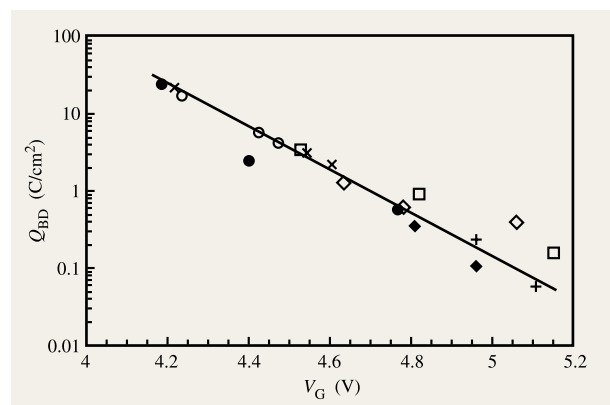


Figure 9

Q_{BD} (63% value) for different processes plotted as a function of applied gate voltage for 2.9-nm oxide (capacitor = $3.14 \times 10^{-4} \text{ cm}^2$). The 63% value corresponds to the zero level in the Weibull distribution $\ln[-\ln(1-F)]$, with F being the cumulative failure rate.

It was also found that, depending on the stress conditions, certain processing steps, such as postimplantation anneals, could either improve or degrade the Q_{BD} value. However, if the data from Figure 8 are plotted as a function of the gate voltage, a single curve, independent of the processing conditions, is obtained. This is shown in Figure 9, where the data for various postimplantation anneals are plotted, together with data for other processing conditions, such as amorphous and poly-Si gates [50, 51], and for two stress polarities. It becomes obvious that these variations have no influence on reliability. This is because injected electrons travel ballistically through ultrathin oxides; their energy at the anode is determined by the total applied voltage instead of the oxide field [52–54]. As a consequence, the electron energy released at the anode, which is believed to be related to the oxide trap-generation rate, then depends directly on the applied gate voltage. Therefore, the observed differences in Q_{BD} are due to the processing-induced differences of the gate voltage required to obtain a fixed stress current density.

Conclusions

Some recent developments in the area of cleaning and thin gate-oxide technology were discussed in this paper. It was shown that the IMEC clean combines an excellent performance and process robustness with a low chemical and DI-water consumption and high throughput. Some relevant aspects of this cleaning concept were discussed in more detail. Ozonated DI water can be used to remove organic contamination, but a careful optimization of the process conditions is needed to enhance the efficiency of

this process. The dilute HF step can be optimized by the addition of HCl to avoid Cu outplating. The effect of the final rinse on the metal surface contamination is often unjustly neglected. Especially for Ca, this step is very important, and rinsing at reduced pH provides lower final contamination levels. The effect of organic contamination and Si surface roughness on the gate-oxide integrity was investigated. Organic contamination is especially damaging when it is deposited on the wafer after the thin oxide growth, prior to the poly-Si deposition. No significant effect of Si surface roughness on gate-oxide integrity was observed when sufficient care was taken to avoid metal contamination. Finally, it was demonstrated that constant-current charge-to-breakdown measurements can lead to erroneous conclusions in assessing the reliability of thin oxide layers.

References

1. W. Kern and D. Poutinen, *RCA Rev.* **31**, 187 (1970).
2. T. Hurd, P. Mertens, H. Schmidt, D. Ditter, L. Hall, M. Meuris, and M. Heyns, *Proceedings of the Institute of Environmental Sciences 40th Annual Technical Meeting*, Vol. 1 (IES, Mount Prospect, IL), 1994, p. 218.
3. T. Hurd, P. W. Mertens, L. Hall, and M. Heyns, *Proceedings of the 2nd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '94*, Acco, Leuven, Belgium, 1994, p. 41.
4. D. Riley and R. Carbonell, *J. Coll. Interface Sci.* **158**, 259 (1993).
5. M. Meuris, P. W. Mertens, A. Opdebeeck, H. F. Schmidt, M. Depas, G. Vereecke, M. M. Heyns, and A. Philipossian, *Solid State Technol.* **38**, 109 (1995).
6. A. F. M. Leenars, J. A. M. Huethorst, and J. J. Van Oekel, *Langmuir* **6**, 1701 (1990).
7. R. Schild, K. Locke, M. Kozak, and M. M. Heyns, *Proceedings of the 2nd International Symposium on Ultra*

- Clean Processing of Silicon Surfaces, UCPSS '94*, Acco, Leuven, Belgium, 1994, p. 31.
8. A. L. P. Rotondaro, H. F. Schmidt, M. Meuris, M. Heyns, C. Claeys, and J. Mulready, *Proceedings of the 2nd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '94*, Acco, Leuven, Belgium, 1994, p. 301.
 9. G. Alder and R. Hill, *J. Amer. Chem. Soc.* **72**, 1884 (1950).
 10. T. Isagawa, M. Kogure, T. Futatsuki, and T. Ohmi, *Proceedings of the Annual Semiconductor Pure Water Conference*, Vol. 12, 1993, p. 117.
 11. *Handbook of Chemistry and Physics*, The Chemical Rubber Publishing Co., Cleveland, OH, 1962, p. 1703.
 12. C. Kenens, S. De Gendt, D. M. Knotter, L. Loewenstein, M. Meuris, W. Vandervorst, and M. M. Heyns, *ECS Proceedings 97-35* (The Electrochemical Society, Pennington, NJ), p. 247 (1997).
 13. S. De Gendt, P. Snee, I. Cornelissen, M. Lux, R. Vos, P. W. Mertens, D. M. Knotter, and M. Heyns, *1998 Symposium on VLSI Technology, Digest of Technical Papers*, 1998, p. 168.
 14. T. Ohmi, T. Imaoka, I. Sugiyama, and T. Kezuka, *J. Electrochem. Soc.* **139**, 3317 (1992).
 15. K. K. Yoneshige, H. G. Parks, S. Raghavan, J. B. Hiskey, and P. J. Resnick, *J. Electrochem. Soc.* **142**, 671 (1995).
 16. H. Morinaga, M. Suyama, and T. Ohmi, *J. Electrochem. Soc.* **141**, 2834 (1994).
 17. I. Teerlinck, P. W. Mertens, M. Meuris, and M. Heyns, *1996 Symposium on VLSI Technology, Digest of Technical Papers*, 1996, p. 206.
 18. I. Teerlinck, P. Mertens, R. Vos, M. Meuris, and M. Heyns, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 21.
 19. H. Schmidt, I. Teerlinck, W. Storm, H. Bender, M. Meuris, P. Mertens, and M. Heyns, *Proceedings of the 4th International Symposium on Cleaning Technology in Semiconductor Device Manufacturing*, The Electrochemical Society, Pennington, NJ, 1995, p. 498.
 20. W. Fyen, L. Mouche, M. Meuris, M. Heyns, and J. Zahka, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 131.
 21. M. Depas, T. Nigam, K. Kenis, M. M. Heyns, H. Sprey, and R. Wilhelm, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 291.
 22. I. Lampert and L. Fabry, German Patent No. DE 42 09 865 C2, June 30, 1994.
 23. L. Fabry, S. Pahlke, L. Kotz, P. Blöchl, T. Ehmann, and K. Bächmann, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 163.
 24. P. W. Mertens, L. M. Loewenstein, R. Vos, S. De Gendt, T. Bearda, and M. M. Heyns, *ECS Proceedings 98-1* (The Electrochemical Society, Pennington, NJ), p. 592 (1998).
 25. S. Verhaverbeke, M. Meuris, P. W. Mertens, M. M. Heyns, A. Philipossian, D. Gräf, and A. Schnegg, *Proceedings of the International Electron Devices Meeting (IEDM)*, Washington, DC, 1991, p. 71.
 26. A. Tonti, *Proceedings of the Second International Symposium on Cleaning Technology in Semiconductor Manufacturing*, **92-12**, The Electrochemical Society, Pennington, NJ, 1992, p. 409.
 27. L. M. Loewenstein and P. W. Mertens, *Proceedings of the Fifth International Symposium on Cleaning Technology in Semiconductor Manufacturing*, **97-35**, The Electrochemical Society, Pennington, NJ, 1998, p. 89.
 28. L. M. Loewenstein and P. W. Mertens, *Proceedings of the 4th International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '98*, Scitec Publications, Switzerland, 1998.
 29. M. M. Heyns, N. Anderson, I. Cornelissen, M. Daniels, M. Depas, S. De Gendt, W. Fyen, T. Hurd, M. Knotter, A. Lubbers, M. J. McGeary, P. W. Mertens, M. Meuris, L. Mouche, M. Schaekers, P. Snee, H. Sprey, I. Teerlinck, J. Van Hoeymissen, V. Vermeire, R. Vos, and J. Zahka, *Proceedings of the Semicon Geneva Technical Session*, Geneva, Switzerland, April 1997.
 30. T. Yoshida, D. Imafuku, S. Miyazaki, and M. Hirose, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 305.
 31. F. Tardif, G. Quagliotti, T. Baffert, and L. Secourgeon, *Proceedings of the 3rd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '96*, Acco, Leuven, Belgium, 1996, p. 309.
 32. T. Ohmi, *J. Vac. Sci. Technol. A* **13**, 1665 (1995).
 33. S. De Gendt, D. M. Knotter, K. Kenis, M. Depas, M. Meuris, P. W. Mertens, and M. M. Heyns, *Jpn. J. Appl. Phys.* **37**, Part I, No. 9A, 4649 (1998).
 34. M. Offenberger, M. Liehr, G. W. Rubloff, and K. Holloway, *Appl. Phys. Lett.* **57**, 1254 (1990).
 35. C. Sofield, M. Murrell, M. Heyns, S. Verhaverbeke, M. Welland, B. Galen, and J. Barnes, in *Chemical Surface Preparation, Passivation and Cleaning for Semiconductor Growth and Processing*, Vol. 259, Materials Research Society, Pittsburgh, 1992, p. 105.
 36. M. Hirose, M. Hiroshima, T. Y. Asaka, and S. Miyazaki, *J. Vac. Sci. Technol. A* **12**, 1864 (1994).
 37. M. Depas, A. Crossley, B. Vermeire, P. W. Mertens, C. J. Sofield, and M. M. Heyns, presented at the 26th IEEE Semiconductor Interface Specialist Conference, Charleston, SC, 1995.
 38. C. J. Sofield and A. M. Stoneham, *Semicond. Sci. Technol.* **10**, 215 (1995).
 39. R. I. Hedge, M. A. Chonko, and P. J. Tobin, *J. Vac. Sci. Technol. B* **14**, 3299 (1996).
 40. M. Depas, M. M. Heyns, T. Nigam, K. Kenis, H. Sprey, R. Wilhelm, A. Crossley, C. J. Sofield, and D. Gräf, *Proceedings of the Third International Symposium on the Physics and Chemistry of SiO₂ and the Si-SiO₂ Interface*, **96-1**, The Electrochemical Society, Pennington, NJ, 1996, p. 352.
 41. M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, "Influence of Extreme Surface Roughness on the Electrical Characteristics of Ultra-Thin Oxides," *Solid-State Electron.* **43**, 159 (1999).
 42. H. F. Schmidt, M. Meuris, P. W. Mertens, A. L. P. Rotondaro, M. M. Heyns, T. Q. Hurd, and Z. Hatcher, *Proceedings of the 2nd International Symposium on Ultra Clean Processing of Silicon Surfaces, UCPSS '94*, Acco, Leuven, Belgium, 1994, p. 259.
 43. H. F. Schmidt, M. Meuris, P. W. Mertens, A. L. P. Rotondaro, M. M. Heyns, T. Q. Hurd, and Z. Hatcher, *Jpn. J. Appl. Phys.* **34**, 727 (1995).
 44. D. M. Knotter, S. De Gendt, P. Mertens, and M. M. Heyns, *Mater. Res. Soc. Symp. Proc.* **477**, 63 (1997).
 45. S. De Gendt, D. M. Knotter, K. Kenis, P. W. Mertens, and M. M. Heyns, *J. Electrochem. Soc.* **145**, 2589 (1998).
 46. T. Nigam, R. Degraeve, G. Groeseneken, M. Heyns, and H. E. Maes, "Is the Constant Current Charge-to-Breakdown Test Still a Valid Tool to Study the Reliability of MOS Structures?" *Proceedings of the IEEE International Reliability Physics Symposium*, 1998, pp. 62-69.
 47. R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, *IEDM Tech. Digest*, p. 863 (1995).
 48. G. Groeseneken, R. Degraeve, J. De Blauwe, P. Roussel, M. Depas, and H. E. Maes, *ECS Proceedings 97-10* (The Electrochemical Society, Pennington, NJ), p. 3 (1997).

49. R. Degraeve, J. De Blauwe, J. L. Ogier, Ph. Roussel, G. Groeseneken, and H. E. Maes, *IEDM Tech. Digest*, p. 327 (1996).
50. T. Nigam, M. Depas, M. M. Heyns, C. Sofield, and L. Mapeldoram, *Materials Reliability in Microelectronics VII, MRS Symposia Proceedings*, Vol. 473, 1997, p. 101.
51. T. Nigam, M. Depas, R. Degraeve, M. M. Heyns, and G. Groeseneken, *Proceedings of the Solid State Devices and Materials Conference (SSDM)*, Hamamatsu, Japan, September 1997, p. 90.
52. M. V. Fischetti, D. J. DiMaria, S. D. Brorson, T. N. Theis, and J. R. Kirtley, *Phys. Rev. B* **31**, 8124 (1985).
53. D. J. DiMaria and M. V. Fischetti, *J. Appl. Phys.* **64**, 4683 (1988).
54. M. V. Fischetti, S. E. Laux, and D. J. DiMaria, *Appl. Surf. Sci.* **39**, 578 (1989).

Received October 1, 1997; accepted for publication July 21, 1998

Marc M. Heyns IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (heyns@imec.be). Dr. Heyns received the M.Sc. degree in electrical and mechanical engineering in 1979 and the Ph.D. degree in 1986, both from the Katholieke Universiteit Leuven, Belgium. In 1986 he joined IMEC, where he is now responsible for a research group working on Ultra Clean Processing Technology, Environment, Safety and Health issues in IC production (ES&H), advanced gate insulators, dielectrics deposited with LPCVD and PECVD, chemical-mechanical polishing (CMP), and EPI deposition.

Twan Bearda IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (bearda@imec.be). Mr. Bearda received the M.Sc. degree at the Twente University of Technology in the Netherlands. He is currently working in the Ultra Clean Processing (UCP) group at IMEC. His areas of interest include the effects of contamination and substrate defects on gate-oxide integrity, yield measurements, and statistical yield analysis.

Ingrid Cornelissen IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (cornelis@imec.be). Ms. Cornelissen graduated as an engineer in chemistry from the Katholieke Industriële Hogeschool Limburg (KIH), Belgium, in 1994; she subsequently joined the UCP group at IMEC, where she works on the development and implementation of wet cleaning technologies.

Stefan De Gendt IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (degendt@imec.be). Dr. De Gendt joined IMEC in 1996. He received his M.Sc. and Ph.D. degrees in chemistry from the University of Antwerp, Belgium, in 1989 and 1996, respectively. Since 1996 he has worked in the UCP group at IMEC; his research interests involve ozone-cleaning technology and analytical metrology for contamination control.

Robin Degraeve IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (degraeve@imec.be). Dr. Degraeve received the M.Sc. degree in electrical and mechanical engineering from the University of Ghent, Belgium, in 1992, subsequently joining the Reliability Physics group at IMEC. In 1998 he received his Ph.D. from the Katholieke Universiteit Leuven, Belgium. His present interests and activities cover hot-carrier reliability issues in MOSFETs, the physics of breakdown phenomena in oxides, and the reliability of ultrathin oxide layers for VLSI technologies.

Guido Groeseneken IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (groeseneken@imec.be). Dr. Groeseneken received the M.Sc. degree in electrical and mechanical engineering in 1980 and the Ph.D. degree in 1986, both from the Katholieke Universiteit Leuven, Belgium. In 1987 he joined IMEC, where he now heads the research group on reliability physics for submicron technologies. His research activities cover nonvolatile memories, the reliability physics of VLSI technology, hot-carrier effects in MOSFETs, time-dependent dielectric breakdown of oxides, and ESD protection and testing.

Conny Kenens IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (kenens@imec.be). Ms. Kenens received her M.Sc. degree in chemistry from the Katholieke Universiteit Leuven, Belgium, in 1992. During the following two years she focused on environmental protection at the same university. In 1995 she joined IMEC, where she is currently working toward a Ph.D. in chemistry.

D. Martin Knotter Philips Research, Eindhoven, Netherlands (knotter@natlab.research.philips.com). Mr. Knotter received the M.Sc. degree in organic chemistry from the University of Amsterdam, Netherlands, in 1986 and began his Ph.D. study at the University of Utrecht. In 1990 he joined the Philips Research Laboratories, where in 1995 he became project leader of Surface Preparation in the Semiconductor Process Modules Department. He is responsible for the coordination of the silicon cleaning activities at Philips and works part-time in the UCP group at IMEC.

Lee M. Loewenstein Texas Instruments, 13500 North Central Expressway, Dallas, Texas 75243 (loewenst@imec.be). Dr. Loewenstein is a Senior Member of Technical Staff at Texas Instruments. His work has centered on isotropic film removal processes and wafer cleaning. Since 1996 he has been TI's assignee to the IMEC UCP program, where he has been studying metal contamination of the silicon surface. Dr. Loewenstein received his Ph.D. in chemistry in 1984 from Harvard University.

Paul W. Mertens IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (mertensp@imec.be). Mr. Mertens is section head of Ultra Clean Processing at IMEC. His research interests involve cleaning technology, silicon wafer quality, novel gate-stack technologies, and manufacturing science. He has authored and coauthored more than 100 scientific and technical papers on the matter and has presented at several international conferences.

Sofie Mertens IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (mertenss@imec.be). Ms. Mertens graduated as an engineer in chemistry, option polymer technology, in 1991. She subsequently joined the UCP group at IMEC, where she works on process development in the furnace and CVD area.

Marc Meuris IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (meuris@imec.be). Dr. Meuris has worked at IMEC since 1984, beginning in the GaAs processing group. In 1986 he joined the analysis group, where he developed SIMS analysis procedures. Since 1990 he has worked in the UCP group, concentrating on cleaning technology. Since 1997 he has also been responsible for the coordination of CMP research at IMEC. Dr. Meuris received his B.S. and Ph.D. degrees in physics from the Katholieke Universiteit Leuven, Belgium, in 1983 and 1990, respectively.

Tanya Nigam *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (nigam@imec.be).* Ms. Nigam received the M.Sc. degree in physics from the Indian Institute of Technology (IIT), Kanpur, in 1994 and a second M.Sc. in electronic engineering from the Katholieke Universiteit Leuven, Belgium, in 1995. Currently she is pursuing her Ph.D. degree in the area of ultrathin oxides in the UCP group at IMEC.

Marc Schaekers *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (schaekers@imec.be).* Dr. Schaekers studied chemistry at the Katholieke Universiteit Leuven, Belgium, where he received his Ph.D. in 1985. After a stay at the University of Wuppertal, Germany, he joined IMEC in 1987. He has been in charge of process development in the furnace and CVD area, primarily on dielectrics deposited with LPCVD and PECVD.

Ivo Teerlinck *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (teerlinc@imec.be).* Mr. Teerlinck graduated as an engineer in chemistry from the Katholieke Hogeschool Limburg, Belgium, in 1994, joining IMEC that same year. In 1996 he received the M.Sc. degree in chemistry from the Universiteit Gent, Belgium, and is currently working toward a Ph.D. degree. His research is primarily directed toward electrochemistry.

Wilfried Vandervorst *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (vdvorst@imec.be).* Dr. Vandervorst received an M.Sc. degree in electrical engineering in 1977 and a Ph.D. in 1983 from the Katholieke Universiteit Leuven, Belgium. From 1983 to 1984 he worked at Bell Northern Research, Ottawa, Canada. In 1984 he joined IMEC, where he is now head of the group responsible for materials characterization. His interests cover fundamental and applied research dealing with materials development and characterization, with an emphasis on ion-solid interactions, doping processes, and scanning probe methods for device characterization. In 1990 Dr. Vandervorst was appointed a Professor at the Katholieke Universiteit Leuven.

Rita Vos *IMEC, Kapeldreef 75, B-3001 Leuven, Belgium (vos@imec.be).* Dr. Vos received the M.Sc. and Ph.D. in physical chemistry at the Katholieke Universiteit Leuven, Belgium, in 1991 and 1995, respectively. She subsequently joined the UCP group at IMEC, where she works in the field of wet cleaning technology.

Klaus Wolke *STEAG MicroTech, Pliezhausen, Germany (100656.757@compuserv.com).* Dr. Wolke studied experimental physics and received his Ph.D. at the University of Münster, Germany, in 1988. He joined the IBM Microelectronics Division at the DRAM manufacturing plant in Germany as a process engineer for dry-etch processes. From 1993 he was section manager for wet processing. In 1995 he became Manager of the Process Application and Development Division at STEAG MicroTech, focusing on the development of critical cleaning processes for the S/C industry.